

GENERAL FRONT END ARCHITECTURE

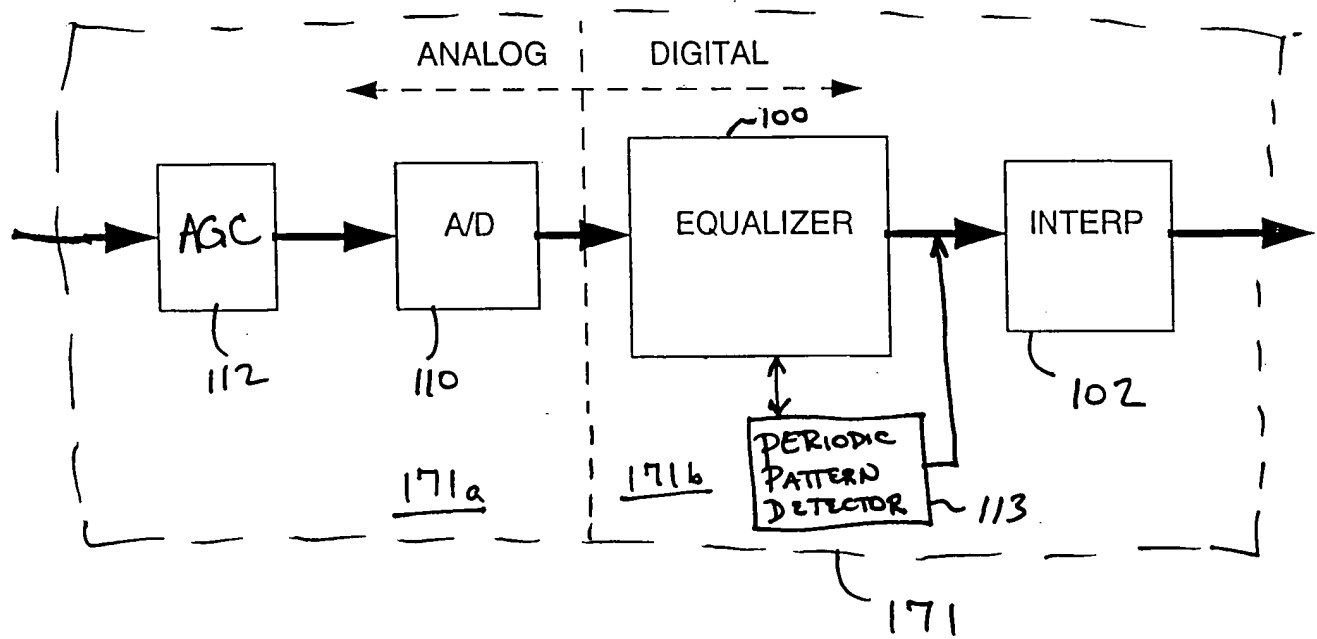


FIG. 1

EQUALIZER ARCHITECTURE

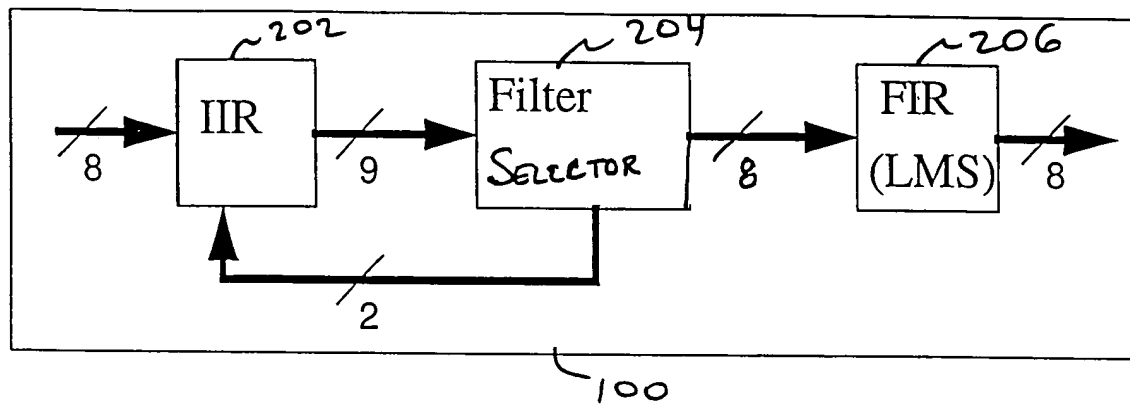


FIG. 2

IIR Filter Block Description

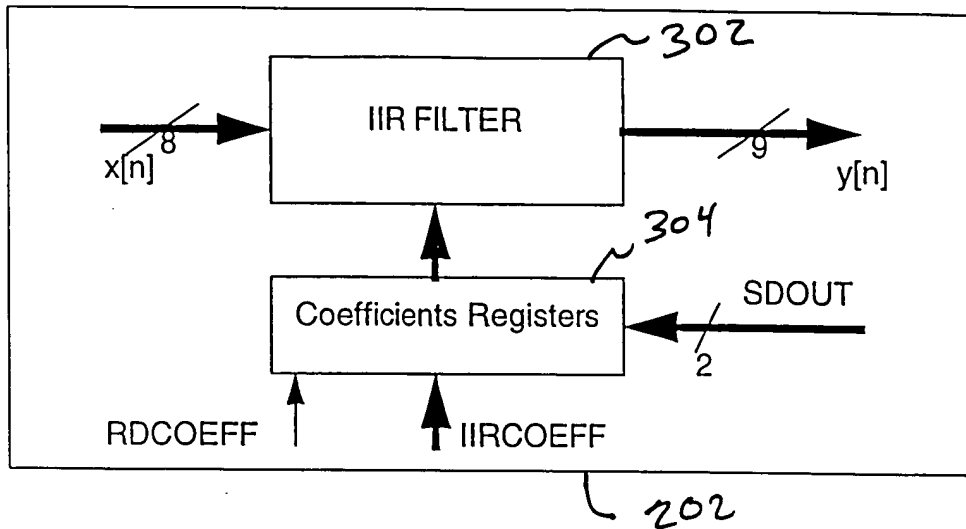


FIG. 3

IIR Filter Block Implementation

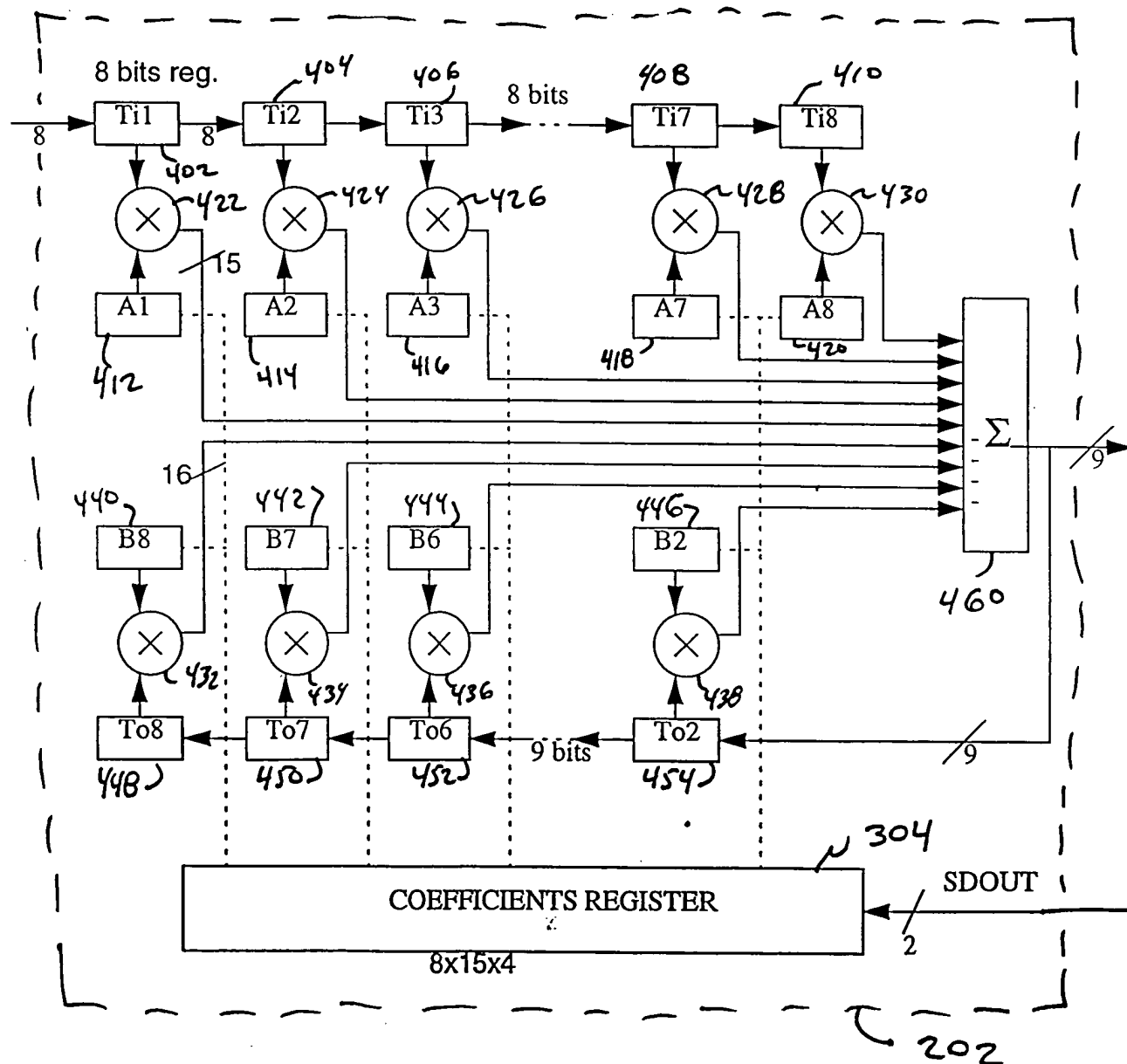


FIG. 4

Filter Selection Block Description

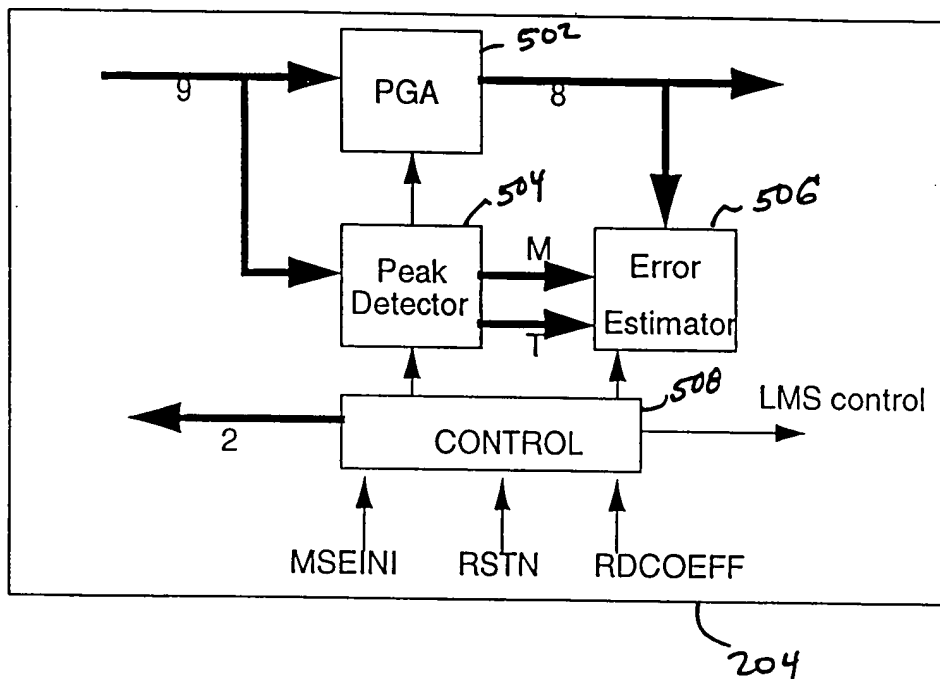


FIG. 5

Filter Selection Block Implementation

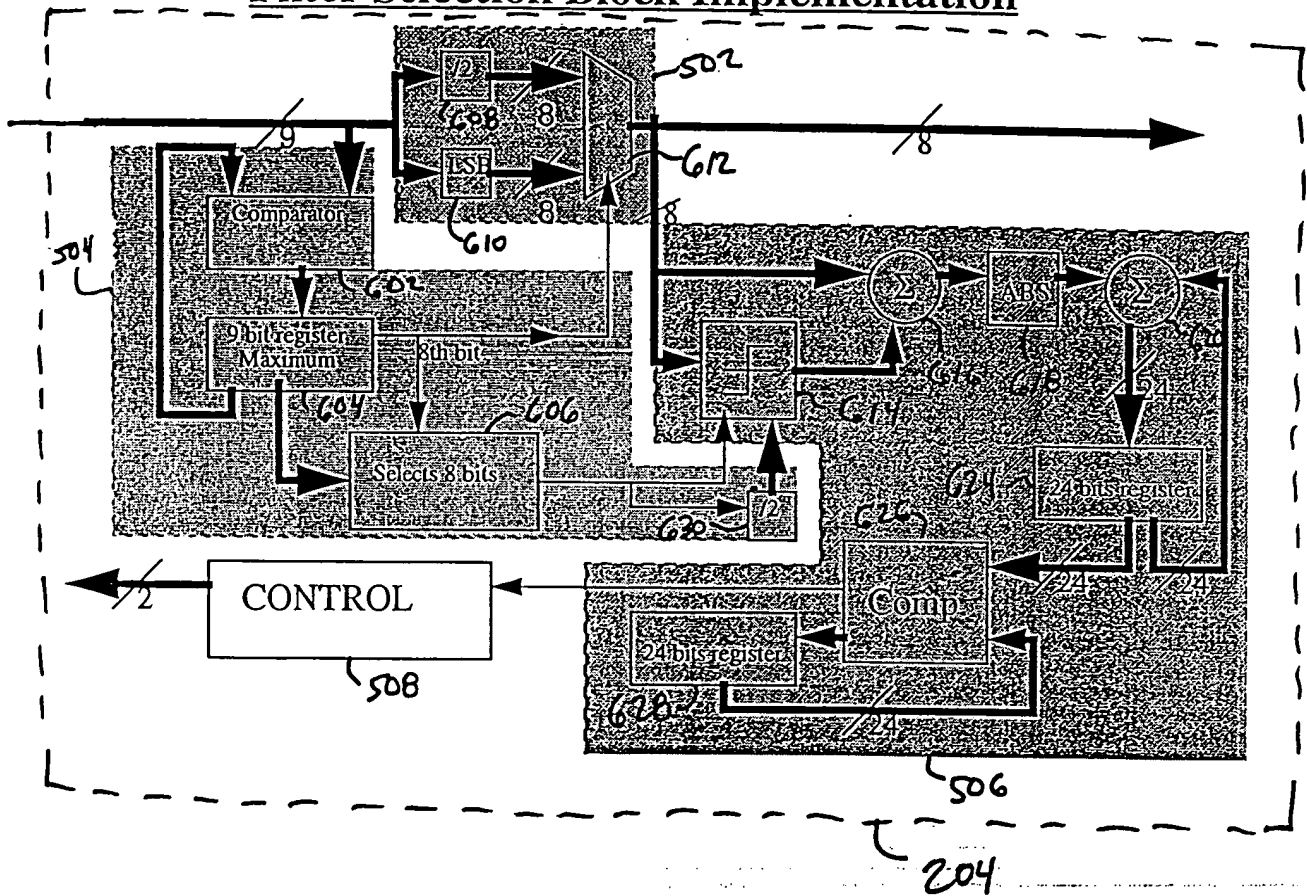


FIG. 6

Adaptive FIR Filter Description

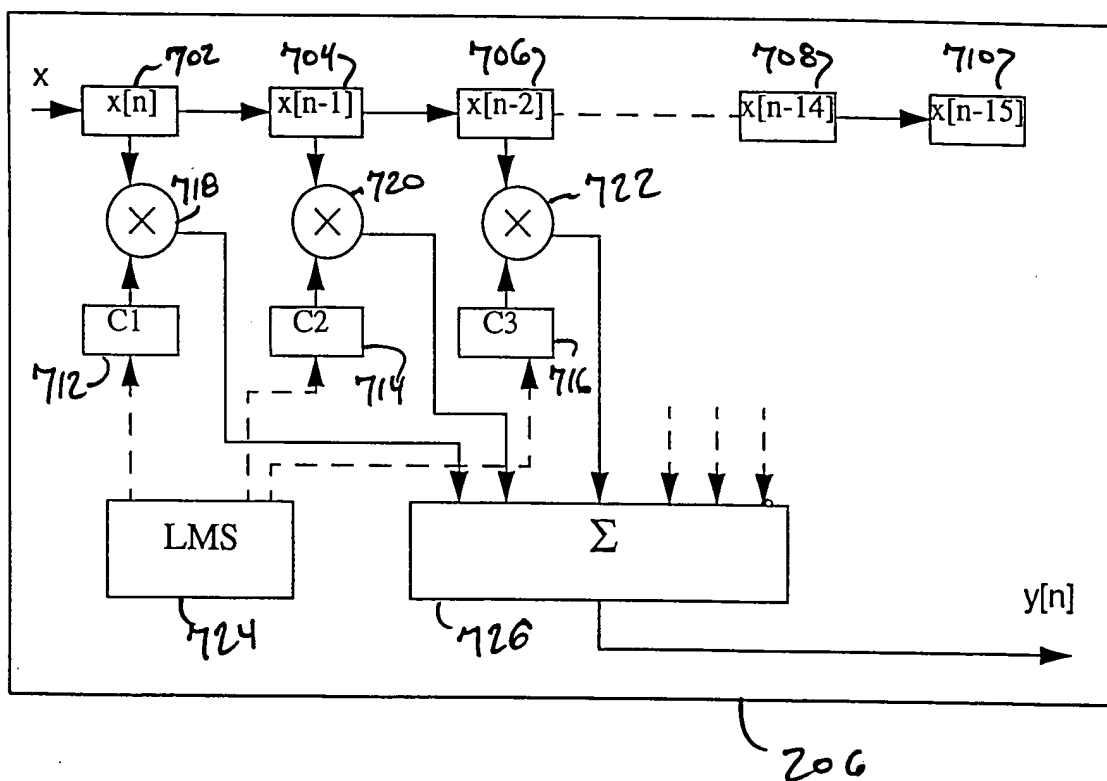


FIG. 7

Adaptive FIR Filter Block Implementation

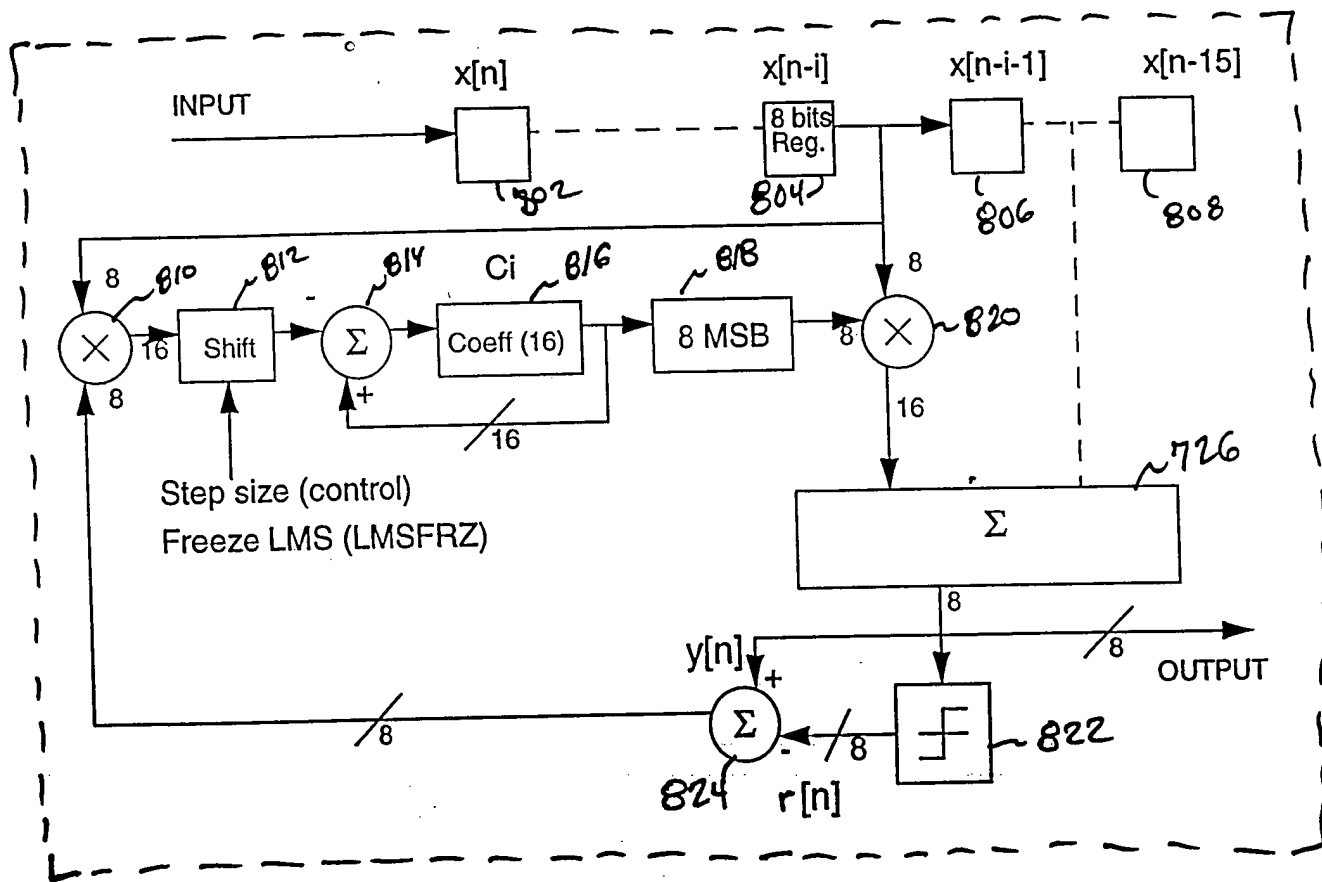
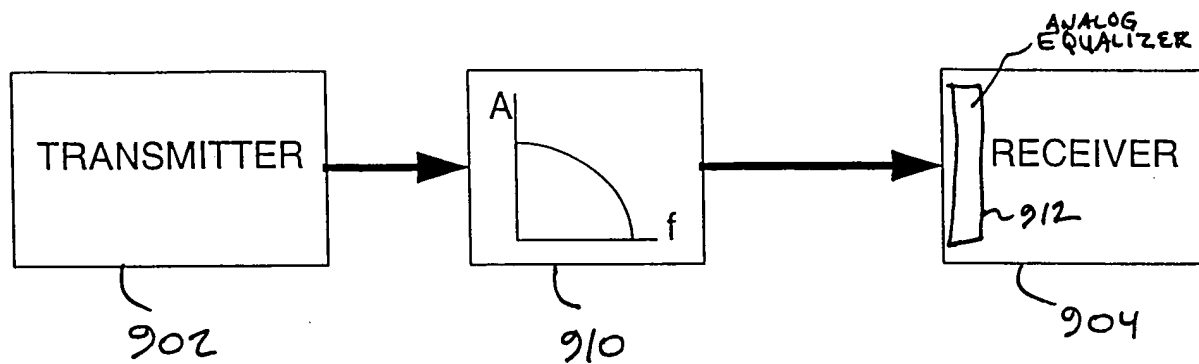


FIG. 8

← T1/E1 CHANNEL →



Prior Art
FIG. 9